

# United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address COMMISSIONER OF PATENTS AND TRADEMARKS

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/848,256	05/04/2001	Kazuyuki Misumi	401188	6322
23548 7	590 05/06/2002			
LEYDIG VOIT & MAYER, LTD			EXAMINER	
700 THIRTEENTH ST. NW SUITE 300			THAI, L	UAN C
WASHINGTO	N, DC 20005-3960		ART UNIT	PAPER NUMBER

2827 DATE MAILED: 05/06/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)					
	09/848,256	MISUMI ET AL.					
Office Action Summary	Examiner	Art Unit					
	Luan Thai	2827					
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet w	vith the correspondence address					
A SHORTENED STATUTORY PERIOD FOR REPLY THE MALLING DATE OF THIS COMMUNICATION.  - Etensions of time may be available under the provisions of 37 CPR 1.13 after SM (6) MONTHS from the mailing date of this communication.  - If NO period for reply is appecified above, the maximum statutory period v - Failure to reply within the set or extended period for reply will, by statute, - Any reply received by the Office later than three months after the mailing earmed patent term adjustment. See 37 CFR 1.704(b).  Status	16(a). In no event, however, may a within the statutory minimum of the fill apply and will expire SIX (6) MC cause the application to become A	reply be timely filed  irty (30) days will be considered timely,  NTHS from the mailing date of this communication  BANDONED (35 U.S.C. § 133).	on.				
1) Responsive to communication(s) filed on							
2a)⊠ This action is <b>FINAL</b> . 2b)□ Thi	s action is non-final.						
Since this application is in condition for allowa closed in accordance with the practice under to Disposition of Claims			is				
4) Claim(s) 4-11 and 16-22 is/are pending in the	application.						
4a) Of the above claim(s) is/are withdraw	n from consideration.						
5) Claim(s) is/are allowed.							
6)⊠ Claim(s) <u>4-11 and 16-22</u> is/are rejected.							
7) Claim(s) is/are objected to.							
8) Claim(s) are subject to restriction and/or	election requirement.						
Application Papers							
9) The specification is objected to by the Examiner							
10) The drawing(s) filed on is/are: a) accep	ted or b) objected to by	the Examiner.					
Applicant may not request that any objection to the	drawing(s) be held in abe	vance. See 37 CFR 1.85(a).					
11) ☐ The proposed drawing correction filed on is: a) ☐ approved b) ☐ disapproved by the Examiner.							
If approved, corrected drawings are required in reply to this Office action.							
12) The oath or declaration is objected to by the Exa	aminer.						
Priority under 35 U.S.C. §§ 119 and 120							
13) Acknowledgment is made of a claim for foreign	priority under 35 U.S.C.	§ 119(a)-(d) or (f).					
a) ☐ All b) ☐ Some * c) ☐ None of:							
<ol> <li>Certified copies of the priority documents</li> </ol>	have been received.						
<ol><li>Certified copies of the priority documents</li></ol>	have been received in	Application No					
Copies of the certified copies of the prior application from the International Bur     See the attached detailed Office action for a list of the certification for a list of the certific	eau (PCT Rule 17.2(a)).	· ·					
14) Acknowledgment is made of a claim for domestic	•		tion				
a) The translation of the foreign language pro-							
15) Acknowledgment is made of a claim for domestic							
Attachment(s)							
Notice of References Cited (PTO-892)     Notice of Draftsperson's Patent Drawing Review (PTO-948)     Information Disclosure Statement(s) (PTO-1449) Paper No(s)		r Summary (PTO-413) Paper No(s) Informal Patent Application (PTO-152)					

U.S. Patent and Trademark Office PTO-326 (Rev. 04-01)

Application/Control Number: 09/848,256

Art Unit: 2827

#### DETAILED ACTION

This Office action is responsive to the amendment filed February 26, 2002.

Claims 4-11 and 16-22 are pending in this application (claims 17-22 are newly added claims).

Claims 1-3 and 12-15 have been canceled.

### Claim Rejections - 35 USC § 112

- 1. The following is a quotation of the first paragraph of 35 U.S.C. 112:
  - The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
- 2. Claims **16 and 21** are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification, as originally filed, does not disclose that each dummy lead extends across one of the longer sides of the semiconductor *chip to reach a position opposite the semiconductor chip*, as recited in claim 16, lines 12-13, and that a part of the semiconductor *chip contacting the surface of the semiconductor chip*, as recited in claim 21, lines 8-9.
- 3. The following is a quotation of the second paragraph of 35 U.S.C. 112:
  - The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 16 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being
indefinite for failing to particularly point out and distinctly claim the subject matter which
applicant regards as the invention.

In claim 16, the expression "each dummy lead extends across one of the longer sides of the semiconductor chip to reach a position opposite the semiconductor chip" is unclear as to which position on the chip is opposite to the chip.

In claim 21, the expression "a part of the semiconductor chip contacting the surface of the semiconductor chip" is confused and not understood as how a part of a semiconductor chip can contact a surface of the semiconductor chip itself.

## Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

 Claims 4-6 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamamura et al. (5.334.803).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 4-6 and 9, Yamamura et al. disclose (specifically see figures 19 and 23-24) a sealed semiconductor device comprising: a semiconductor chip 2; a lead frame including internal leads 4 extending across part of and spaced from a surface of the chip, wherein at least one of the internal leads includes a protrusion protruding toward and contacting the surface of the semiconductor chip at a peripheral area of the chip, and wherein the protrusion is an end of at least one of the internal leads that includes a bend proximate the end.

 Claims 10, 17, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Tomita et al. (5,535,509).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 10, 17, and 19, Tomita et al. disclose (see specifically figures 21-25 and 29-30) a sealed semiconductor device (figures 1A-1B) comprising: a semiconductor chip 2; a lead frame including internal leads 3 extending across part of and spaced from a surface of the chip; a die pad 110 (figures 29-30) on which chip 2 is mounted, wherein the lead frame includes protrusions 111-112 extending substantially perpendicular to and contacting the die pad 110 (see figures 29-30) but not contact the semiconductor chip 2. Tomita et al. further disclose the die pad 110 being substantially rectangular (see figures 29-30) and the protrusions extending proximate a pair of shorter sides of the die pad 110.

Application/Control Number: 09/848,256

Art Unit: 2827

8. Claim 11 is rejected under 35 U.S.C. 102(b) as being anticipated by Aoki (5.834.691).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claim 11, Aoki discloses (see specifically figures 1-7) a sealed semiconductor device comprising: a semiconductor chip 6; a lead frame 10 including internal leads 1 extending across part of and spaced from a surface of the chip (see figures 6a-6d); a die pad 3 on which chip 6 is mounted, wherein the die pad including fixed protrusions 4 extending toward and contacting some of internal leads.

Claims 20-22, insofar as in compliance with 35 USC 112, are rejected under 35
 U.S.C. 102(b) as being anticipated by Lee (5,358,906).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 21-22, Lee discloses (see specifically figures 3-4-5) a sealed semiconductor device comprising: a semiconductor chip 31; a die pad 34a on which the chip is mounted; a lead frame 34 including internal leads 34b extending across part of and spaced from a surface of the chip and electrically connected to electrode pad 32 of the chip via wires 35; a tape member 33 having a first surface to which the internal leads are entirely bonded and fixed, and a second surface not fixed to but contacting the semiconductor chip, to ensure a

fixed distance between the chip and the internal leads; an encapsulating 36 sealed the semiconductor chip.

## Claim Rejections - 35 USC § 103

- 10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- Claims 7 and 16, insofar as in compliance with 35 USC 112, are rejected under
   U.S.C. 103(a) as being unpatentable over Yamamura et al. (5,334,803).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claim 7, it appears from Yamamura et al.'s figure 20 that some of inner leads 4 are not electrically connected to the electrode pads 3 by wirings 5, and thus, it would be obvious for these inner leads to be considered as the claimed of "a dummy internal lead not connected by a wire to the chip".

Regarding claim 16, Yamamura et al. disclose (specifically see figures 19 and 23-24) a lead frame for a sealed semiconductor device comprising: a semiconductor chip 2 having a substantially rectangular shape with a pair of longer sides and a pair of shorter sides and sealed in an encapsulating resin, the lead frame comprising: internal leads 4 extending toward and electrically connected with wires 5 to respective pads 3 located approximately along a

central axis of the semiconductor chip 2; at least one internal lead in direct contact with a surface of the semiconductor chip to ensure a fixed separation between the semiconductor chip and the internal leads, wherein each internal leads extends across one of the longer sides of the semiconductor chip to the corresponding pad, and the at least one internal lead extends across one of the longer sides of the semiconductor chip to reach a position opposite the semiconductor chip. Yamamura et al. do not explicitly disclose the at least one internal lead contacting the surface of the chip being call dummy lead.

It appears from Yamamura et al.'s figure 20 that some of inner leads 4 are not electrically connected to the electrode pads 3, and thus, it would be obvious for these inner leads to be considered as the claimed of "a dummy internal lead". Further, the labels nonetheless are meaningless. The Yamamura et al.'s structure anticipates Applicant's claimed structure regardless of whether some of internal leads are labeled "dummy". See *In re Pearson*, 181 USPQ 642; Fx parte Minks 169 USPQ 120; or *In re* Swinehart 169 USPQ 226, all of which make it clear that mere "labels" or "statements of in intended use" as we have here in "dummy" do not distinguish over Yamamura et al.'s structure which may be likewise labeled.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over
 Yamamura et al. (5,334,803) in view of Nakamura et al. (6,060,770).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claim 8, Yamamura et al. disclose(s) all the limitations of the claimed invention as detailed above except for the dummy internal lead extending toward the chip along and across one of the shorter pair of sides of the chip.

Nakamura et al. while related to a similar Lead-on-Chip design teach (see specifically figure 28) a rectangular shaped semiconductor chip 2 having dummy inner lead portions 5a extending toward the chip along and across one of the shorter pair of sides of the chip 2 (Col. 9, lines 16+). Thus, a dummy lead extending toward the chip along and across one of the shorter pair of sides of the chip is conventional in semiconductor art, specifically in semiconductor lead-on-chip art as taught by Nakamura et al. above. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply Nakamura et al.'s teachings to Yamamura et al. device by forming a dummy lead extending toward the chip along and across one of the shorter pair of sides of the chip since such arrangement structure of dummy lead in a device package is conventional in the art as taught by Nakamura et al.

 Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tomita et al. (5,535,509) in view of Aoki (5,834,691).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claim 18, Tomita et al. disclose(s) all the limitations of the claimed invention as detailed above except for the protrusions extending proximate a pair of longer sides of the rectangular die pad. Note that Tomita et al. do disclose the protrusions extending proximate a pair of shorter sides of the rectangular die pad.

Aoki while related to a similar lead-on-chip with die pad structure design teaches (see specifically figures 25c-25d) the protrusions (S) extending proximate a pair of either shorter sides or longer sides of the rectangular die pad (D). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the die pad of Tomita et al.'s lead frame by forming the protrusions extending proximate a pair of longer sides of the rectangular die pad instead of extending proximate a pair of shorter sides of the rectangular die pad, since such structure is conventional in the art, as taught by Aoki, and the modification is held to be within a general skill of a worker in the art.

#### Conclusion

- 14. Applicant's arguments with respect to claims 4-11, 16 and newly added claims 17-22 have been fully considered, but they are deemed to be moot in view of the new grounds of rejection.
- 15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action because the underlined portions of claims **4-11**, **16** and newly added claims **17-22** raise new issues that would require further consideration and/or search. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is (703) 308-1211. The examiner can normally be reached on 7:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Luan Thai April 30, 2002

DAVID L. TALBOTT SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 2800